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Improving the performance of power MOSFETs by tailoring the driver to the specific MOSFET gate requirements.

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ABSTRACT

An ideal power MOSFET, would have very short transition times, near zero $r_{DS(on)}$, and infinite power handling capability. These characteristics depend largely on the device physics and technology, but no matter how good the device is, there is still a requirement to drive the power MOSFET. There is also a need to match the driver capabilities to those of the MOSFET to achieve the best switching and conduction performance. A low $r_{DS(on)}$ device may be let down by the capability of the MOSFET driver, which generally needs a higher drive capability. This paper outlines a new Vishay Siliconix range of integrated MOSFETs and drivers, developed in power packages, which use optimised silicon and package technologies to provide the most favourable solution for point of load converters.

INTRODUCTION

The power MOSFET driver is often neglected during the design of the power supply, with the power MOSFET being considered the most important part of the switching element. However, it is the driver part of the power system that can sometimes be easily improved to increase the efficiency and switching performance of the power supply. Simply by matching the characteristics of the driver to that of the MOSFET, it is possible to improve the performance of the MOSFET, and as such the performance of the power supply. There is also a requirement (or opportunity) to match the driver and MOSFET to specific applications, such as point of load (POL) topology, where a low voltage and high current is required, derived from a relatively low input voltage in the form of a distributed bus. Typically the distributed bus input into the POL converter (synchronous buck) is either 12 V or 5 V and this is converted into output voltages, which can be as low as 0.9 V, resulting in very small duty ratios. Therefore a synchronous buck converter must have different high-side and low-side switch characteristics to obtain the best performance from the converter. Combining these devices with an integral driver results in an application-specific synchronous buck power stage, which requires just a logic input to control the output voltage and leads to an efficient dc-to-dc power supply.

This paper explores the performance advantages of tailoring both the driver and MOSFET combination to a specific application (Figure 1) and also the benefit of implementing these in an integrated package, with reduced inductance and increased power handling. Efficiency measurements are presented for one specific application to illustrate the advantages of using the integrated driver and power MOSFET package.

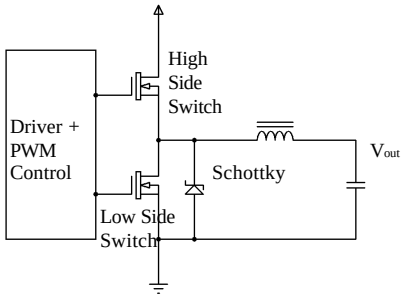


Figure 1. Typical POL synchronous buck schematic.

TYPICAL POINT OF LOAD APPLICATION

A typical POL synchronous buck converter operation condition of a 12-V input and a 1.5-V output results in a duty cycle requirement that could be as low as 12.5%. This dictates the physical size of the silicon for the high-side and low-side devices to be completely different. The size of the silicon for the low side device would need to be large to provide a small $r_{DS(on)}$, whereas the high-side device should be small to enable faster switching times and hence smaller switching losses. There are other POL applications, where the input voltage is closer to the output voltage, resulting in higher duty cycles. In these cases the size of the silicon for both devices needs to be very similar. Therefore for a given process technology, MOSFET cell density and specific available area of silicon, it is best to scale the high-side switch and low-side switch accordingly. Figure 2a shows an analysis of a synchronous buck converter with a 12-V input and a 1.5-V output and how the efficiency varies with different die size ratios between high-side and low-side MOSFET area, where the x-axis is the ratio of silicon for a specific given total area. In this case the die size ratio is defined as being normalised to the low-side device silicon. As the die ratio increases, switching losses become dominant and

progressively reduce efficiency. As the die ratio decreases, conduction losses tend to drive the efficiency lower. The optimum high-side-to-low-side silicon ratio in terms of efficiency for this case is 0.5:1.0. Figure 2b shows the same analysis for the same amount of total silicon area, but with a higher input voltage level of 20V. In this instance the ideal ratio of high-side silicon area to low-side is 0.3:1.0. By knowing this, it is possible to maximize the low-side silicon area for the appropriate current level and then scale the high-side device area accordingly. For high duty cycle applications, such as POL converters with low input voltages , the ideal die ratio is 1.0:1.0.

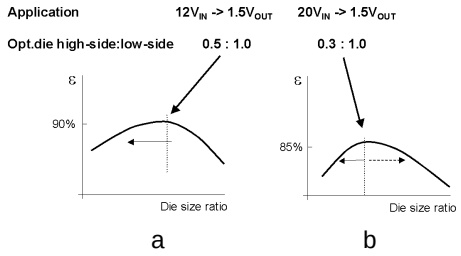


Figure 2. Effect of die ratio on efficiency.

THE DRIVER TECHNOLOGY

Gate-driver timing and associated dead times

Switching losses in a dc-to-dc converter can be classed as consisting of two elements: gate drive losses and the losses associated with the voltage and current switching transient of the MOSFET. However, in a synchronous buck converter there is also the possibility of cross-conduction losses, which can occur at the two transitions during the switching cycle of the power supply, as shown in Figure 3.

If the delay time between the high-side and low-side gate signals is not sufficiently long enough to take account of the delays and transients associated with the MOSFET switching then cross conduction occurs. In this situation both devices will conduct and hence there will be a low-resistance path between the applied input voltage and ground resulting in losses.

For the high-side turn-off to low-side turn-on delay time, it has been found that the most reliable and efficient way of controlling this is through adaptive switching, which ensures that the high side is turned-off before the low side is turned on. as shown in Figure 4. The low-side device will not turn on until the voltage at the MOSFET half-bridge mid-point (Figure 1) is less than a predefined voltage , thereby ensuring that the high-side device is already off.

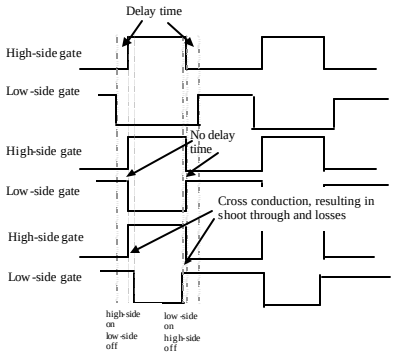


Figure 3. Timing of the high-side and low-side gate signals illustrating cross conduction

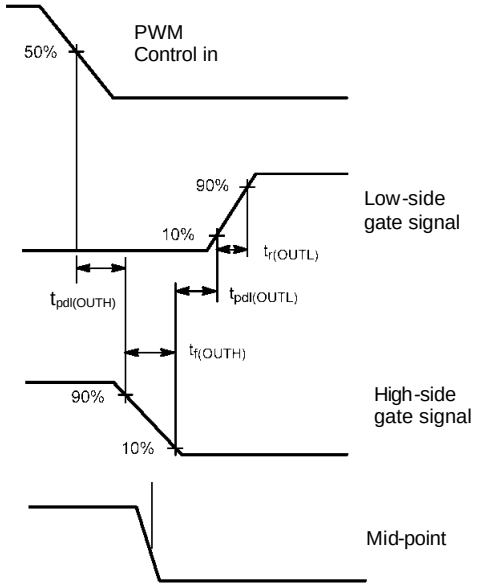


Figure 4. Adaptive high-side turn-off low-side turn-on control.

The low-side turn-off high-side turn-on can be controlled through adaptive switching, but an improvement in efficiency can be achieved by instead using a fixed delay time. This is because the low-side body diode, if allowed to conduct, significantly increases the losses in the switchmode power supply (SMPS), which are related to the Q_{rr} and the V_f of the diode. The losses associated with the Q_{rr} are directly related to the reverse recovery performance of the body diode and proportional to the switching frequency. If the body diode is in conduction for a relatively long time, due to excess dead time, then there will be an

increase in the conduction losses due to the V_f of the body diode. However, it is the Q_{rr} that will generally contribute more to the losses than the V_f, since the dead time (and hence the time the diode is forward biased) is usually a very small percentage of the on-time of the MOSFET (<1%). The body diode is prevented from going into conduction. By reducing the low-side-to-high-side turn-on, dead time is kept to an absolute minimum allowing total non-conduction of the body drain diode. The improvement with efficiency, due to the reduction of the dead-time, is shown in Figure 5.

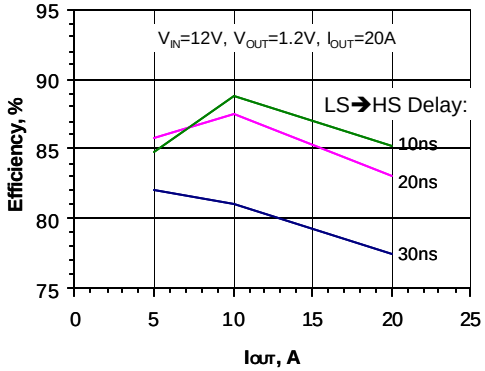


Figure 5. Simulation showing the improvement in efficiency with the reduction of dead time.

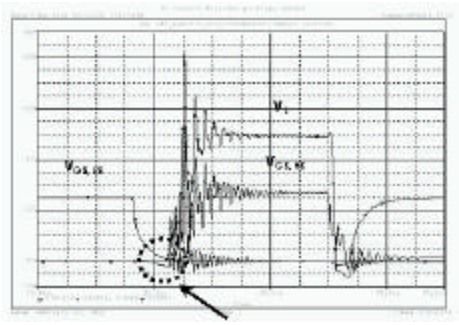
The reduction of the delay time does have the disadvantage of causing cross conduction; however, as long as this period is controlled, this will not be an issue. Since the MOSFET and driver are integrated, the chip designers can achieve an accurately controllable dead time geared towards the available MOSFET silicon. A secondary effect, caused by the introduction of a small cross-conduction period, is shown in Figures 6a and b. Here it is seen that the peak ringing voltage is reduced by the cross-conduction condition. This limits the voltage stress on the MOSFET, allowing designers to possibly use a lower V_{DS}-rated MOSFET for improved performance or reduced cost.

SILICON TECHNOLOGY

Lower gate threshold MOSFETs

With dedicated power MOSFETs and drivers in one package it is possible to optimise the silicon to the final application. One such optimisation is to use a low-side MOSFET with a low gate threshold, (V_{th}). This has three effects on the performance of the MOSFET as shown in Table 1. A low V_{th} slows down the turn-off of the MOSFET and in doing so allows some cross-conduction, which helps to dampen the ringing of the voltage seen on the mid-point of the MOSFET bridge. Also a low gate threshold results in lower conduction losses due to the associated lower $r_{DS(on)}$, and the turn-on rise time is reduced with a lower V_{th}.

a. Without cross conduction



b. With cross conduction

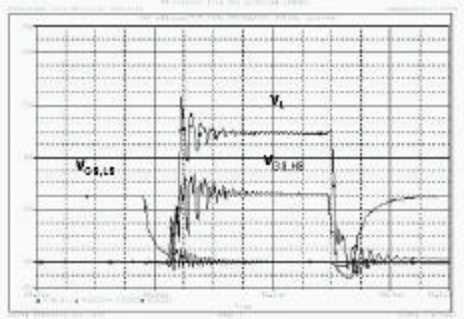


Figure 6. The effects of cross conduction on the peak ringing value of the mid-point.

Event	Issue	Parameters	Effects
Turn-off	Ringing	$t_f = r_G C_{iss} / V_{th}$	Allows longer turn-off time
Turn-on	Body diode	$t_r = r_G C_{iss} / (V_{GS}-V_{TH})$	Reduces rise time
Conduction	Low r_{DS}	$r_{DS} \sim 1 / (V_{GS}-V_{th})$	Lower R

Table 1. Summary of the effects of a low gate threshold.

Lowering the threshold of the MOSFET can be done in one of two ways:
1) lowering the doping or
2) by using a thin the gate oxide.

Lowering the doping requires a longer channel length to help maintain sufficient charge to prevent punch-through:

$$Q_{ch} = N_{dop} * L_{ch}. \quad (1)$$

Increasing the channel length increases the C_{iss} and $r_{DS(on)}$ of the MOSFET.
Thinning the gate oxide will result in an increase in the capacitance:

$$C_{iss} \text{ and } C_{rss}: C_{gx} = e / T_{ox} \quad (2)$$

Thus, this can increase switching losses when used at frequencies above 300 kHz. However, for low-frequency applications with low gate-drive voltage, say 300 kHz and 5 V, a lower-gate-threshold device can offer better performance.

DV/DT shoot through rugged

The silicon can also be optimised to provide a device that is shoot-through rugged. This condition occurs when the high side turns on, causing a high dV/dt transition on the switching node (mid-point). This sharp rise in voltage can inflict a voltage pulse on the low-side MOSFET gate due to the Miller capacitance feedback (Figure 7). If the gate threshold is low then the occurrence of this condition can be more frequent and as such more of a concern for the designer than a MOSFET with a relatively high gate threshold value. However, proper selection of MOSFET parameters and optimisation of the MOSFET process can help reduce this effect. By controlling the ratio of the capacitances involved in this feedback mechanism (C_{gd} and C_{gs}), the V_{GS} pulse may be limited by the equation

$$V_{GS}(t_0) = R_G * C_{rss} * \frac{V_{DS}}{t_o}\left(1 - e^{\frac{-t_0}{R_G * C_{iss}}}\right) \qquad \textbf{(3)}$$

For a set condition, a family of curves can be generated (Figure 8) to prevent shoot through during this switching transient. For example, with a C_{iss}=4 nF, the C_{rss}/C_{iss} ratio needs to be less than 0.4 (Q_{gd}/Q_{gs} ratio of 1.0) for a typical threshold of 1.8 V to 2 V. Use of a low-threshold MOSFET requires a ratio of less than 0.25 (Q_{gd}/Q_{gs} ratio of 0.8) to ensure that shoot-through is minimised.

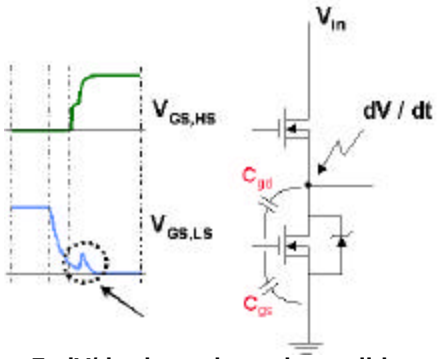


Figure 7. dV/dt shoot-through condition

High cell density

New MOSFET processing technologies have been developed to lower the MOSFET $r_{DS(on)}$, reduce switching losses, and lower Q_{GD}. The first process improvement was to increase the cell density and reduce the trench depth. Increasing the density requires a narrower trench and thus a reduction in the Q_{GD}. The increased cell density[1] also allows for more parallel trenches and a reduction in the MOSFET resistance per area. For comparison, previous MOSFET technology for an SO-8 package yielded an $r_{DS(on)}$-Q_G figure of merit of 240 m?-nC, with a maximum r_{DS} at 4.5 V and typical Q_G at 4.5 V. The higher-cell-density $r_{DS(on)}$-Q_G figure of merit is 110 m?-nC.

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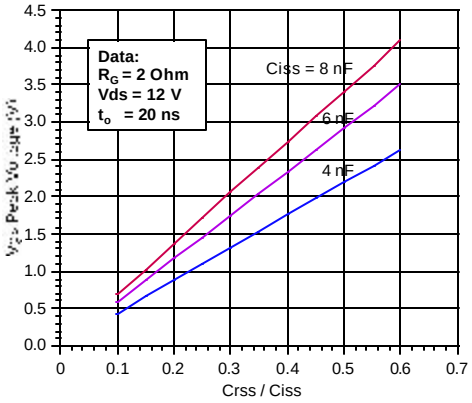

Figure 8. Shoot through ruggedness curves.

PACKAGE TECHNOLOGY

Vishay Siliconix initially developed an SO-16 package to house the integrated driver and MOSFETs. iThe development of new silicon technology and a further understanding of the requirements has resulted in a family of SO-16 devices that include the integration of a Schottky diode with the low-side MOSFET (Si4724CY) and two sets of MOSFET voltage ranges: 30 V (Si4768CY) and 20 V (Si4770CY). The SO-16 package and product efficiencies tend to limit the maximum current to 15 A, with a switching frequency of 200 kHz. To extend this current range the SO-16 parts have been configured to be used in multi-phase power supplies, and a 4-phase evaluation board has been built and is shown in Figure 9.

To provide a part with a higher current capability of at least 20 A at a switching frequency of 1 MHz per phase, a change in package was required. Therefore a thermally enhanced package has been developed, which maintains a small board area, whilst increasing the thermal performance, in the form of a 9 mm by 9 mm MLF package (Figure 10). This package also lends itself to further improvements on the internal construction and

by reducing the lead inductance significant efficiency improvement can be made, as shown in Figure 11, which shows this step-wise efficiency improvement using simulations.

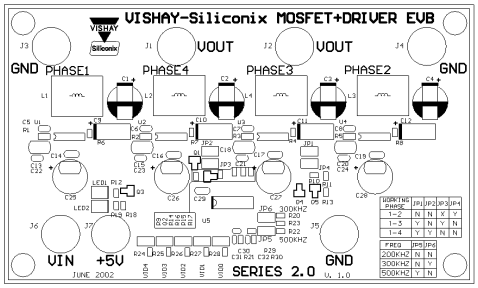

Figure 9. Four-phase evaluation board, implementing SO-16 packages.

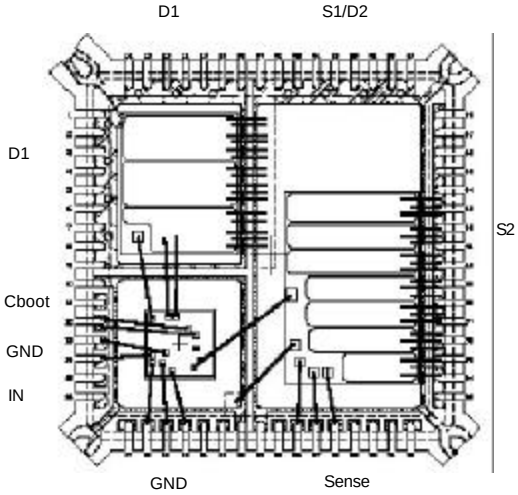

Figure 10. Schematic of new MLF package.

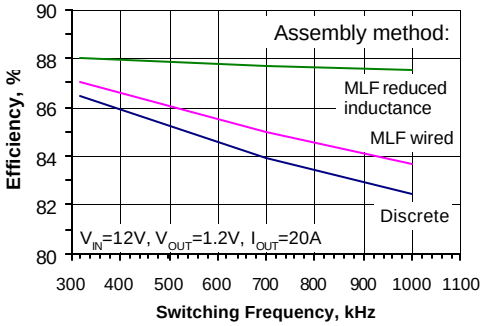

Figure 11. Simulations showing improvement in efficiency with packages.

TEST RESULTS

Using the four-phase board shown in Figure 9 (available from Vishay Siliconix), several tests were completed to obtain a trend of the performance of the integrated driver and MOSFETs in the SO-16 package (Si4770CY) and these are shown in Figures 12 through to 16. The most efficient measurement was nearly 96% at a 5-A load and device switching frequency of 500 kHz. An interesting phenomenon is the low efficiency of the devices at 200 kHz at low loads (Figures 12 and 13). This effect is probably caused by the lossy magnetics (designed for higher currents) and the circuit efficiency at 200 kHz does improve with higher loads.

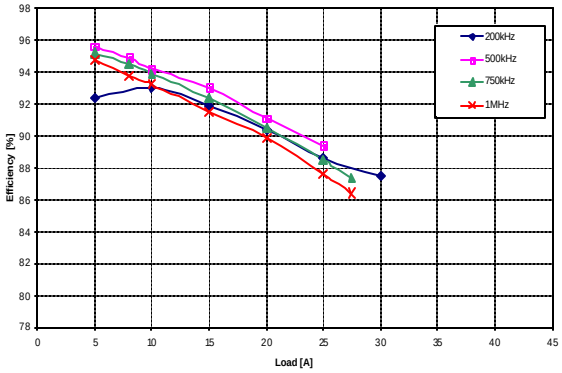

Figure 12. Efficiency of the Si4770CY with 12 Vin 1.85 Vout.

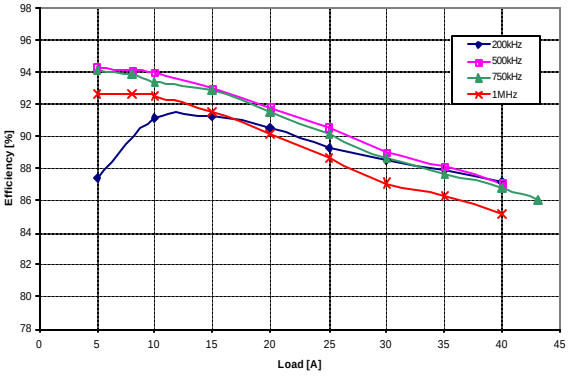

Figure 13. Efficiency of the Si4770CY with 5 Vin, 1.85 Vout.

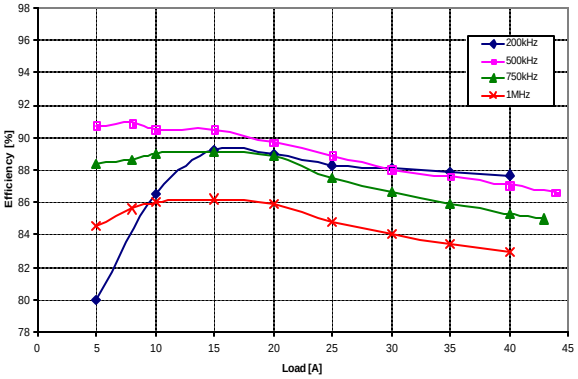

Figure 14. Efficiency of the Si4770CY with 12 Vin, 1.85 Vout.

The Si4770CY is designed to be more efficient at low duty cycles, according to Figure 2. However, it can be seen from Figures 15 through to 17 that efficiency under higher-duty test conditions is greater than at low load currents (<25 A). This is purely due to the low duty cycle test condition having a relatively high input voltage and hence higher switching losses, due to the conduction losses not being as dominant as the switching losses at low load. This is shown in Table 2, where simple analytic loss equations [2] are used to give a trend of the losses in the synchronous buck converter.

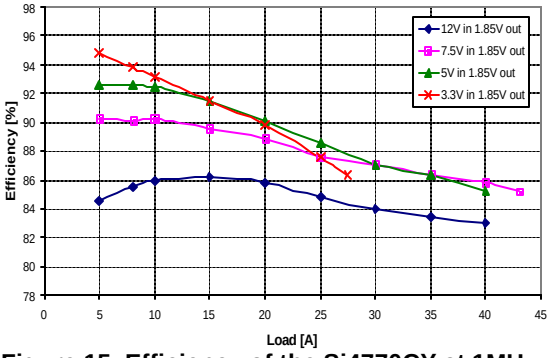

Figure 15. Efficiency of the Si4770CY at 1MHz

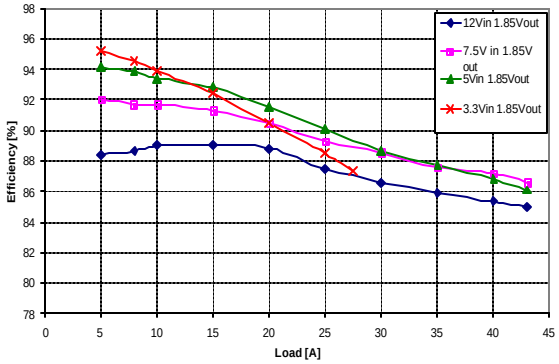

Figure 16. Efficiency of the Si4770CY at 750kHz

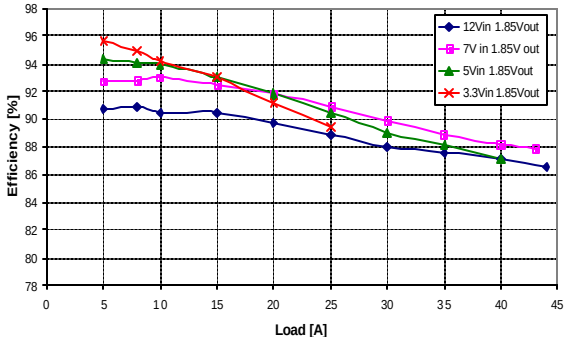

Figure 17. Efficiency of the Si4770CY at 500kHz

Load [A]	Vin 12V	5V	3.3V
Conduction Losses			
10	0.17	0.19	0.21
20	0.73	0.82	0.91
30	1.80	1.99	2.25
40	3.63	3.96	4.63
Switching Losses			
10	1.77	1.26	0.60
20	2.64	1.63	1.38
30	3.51	1.99	1.62
40	4.38	2.35	1.86
Total losses			
10	1.94	1.46	0.81
20	3.37	2.44	2.29
30	5.31	3.98	3.87
40	8.01	6.31	6.48

Table 2. Losses calculated using analytic equations.

CONCLUSIONS

Integrated MOSFET and driver products can bring a performance improvement for dc-to-dc synchronous buck power supplies. This paper has shown that SO-16 MOSFET integrated devices offer excellent efficiency for POL applications. In addition, the 9 mm by 9 mm MLF packaging will provide an unsurpassed performance in delivering 20 A per device at a switching frequency of 1 MHz. The optimisation of the die size ratio, dead-time control, and MOSFET plus driver provides the best solution for the synchronous buck converter but care should be taken to ensure that the circuit is designed for the specific application. In general fast switching devices should be used for the high side and low $r_{DS(on)}$ devices used for the low side. Therefore, with the drive for increased efficiency there will be a trend for more MOSFETs, and/or integrated MOSFETs, which are designed to be specifically suited to the circuit requirements, with a range of products covering multiple applications.

References

[1] Ultra High Cell Density TrenchFET devices: Obtaining that Critical Balance of Switching Performance Verses On Resistance and its Associated Impact on Device Selection. Guy Moxey, PCIM proc. Nuremberg 2002.

[2] Jess Brown, Serge Jaunay, 'DC to DC Design Guide', Application Note AN607, 10th October 2002 Document Number 71917, (http://www.vishay.com/document/71917/71917.pdf).